AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

[0015] The present invention, among other applications, is directed to solving these and other problems and disadvantages of the prior art. The present invention provides a superior technique for providing application programs with the ability to embed native instruction sequences for execution by a microprocessor. In one embodiment, an apparatus is provided in a microprocessor for executing native instructions that are provided directly to the microprocessor via an external instruction bus. The apparatus includes instruction translation logic and bypass logic. The instruction translation logic retrieves macro instructions provided via the external instruction bus, and translates each of the macro instructions into associated native instructions for execution. If a first form of a first macro instruction is retrieved, the instruction translation logic directs the microprocessor to enable a native bypass mode and indicates such by asserting a first bit within a control register. The bypass logic is coupled to the instruction translation logic. The bypass logic accesses the first bit within the control register to determine if the native bypass mode has been enabled, and detects wrapper macro instructions and, upon detection of the wrapper macro instructions, disables the instruction translation logic, and provides the native instructions for execution by the microprocessor, thereby bypassing said instruction translation logic. The wrapper macro instructions are existing macro instructions which are translated by the instruction translation logic according to architectural specifications if the native bypass mode has not been enabled.

[0016] One aspect of the present invention contemplates an apparatus, for allowing a micro instruction to be directly provided from an external instruction bus to execution logic within a pipeline microprocessor. The apparatus has a translator and bypass logic. The translator receives macro instructions from a macro instruction bus, and translates each of the macro instructions into associated micro instructions, the associated micro instructions being provided to the execution logic via a micro instruction bus. The

bypass logic is coupled to the translator, and routes the micro instruction to the execution logic. The bypass logic includes a mode detector and native instruction routing logic. The mode detector detects a native bypass mode, and detects a wrapper macro instruction, and directs that the translator cease instruction translation, where the wrapper macro instruction is an existing macro instructions which would otherwise be translated by the translation logic according to architectural specifications if the native bypass mode is not enabled.. The native instruction routing logic is coupled to the mode detector. The native instruction routing logic receives the wrapper macro instruction from the macro instruction bus, and provides the micro instruction to the micro instruction bus, thereby circumventing the translator.

[0017] Another aspect of the present invention comprehends a method for providing a plurality of native instructions stored in a memory directly to a microprocessor for execution. The method includes enabling a native instruction bypass mode within the microprocessor; embedding the plurality of native instructions within a corresponding plurality of wrapper instructions and providing the corresponding plurality of wrapper instructions to the microprocessor, where the corresponding plurality of wrapper instructions are existing macro instructions, and where the corresponding plurality of wrapper instructions would otherwise be translated by instruction translation logic according to architectural specifications in the absence of the enabling; and within the microprocessor, detecting the native instruction bypass mode and extracting the plurality of native instructions from within the corresponding plurality of wrapper instructions.